A FRONT-END STAGE FOR NEURAL SIGNAL RECORDING BASED ON A SIGMA-DELTA MODULATOR

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Keywords: Neural signal recording, Low noise amplifier.

Abstract: A new device for peripheral neural signals recording is presented. The designed system is composed by an analog and a digital part. The analog part, to be integrated on an implantable CMOS chip, is kept as simple as possible and hosts a low noise first order pre-amplifier/pre-filtering stage that provides a $46dB$ gain in the bandwidth $800Hz - 7.2kHz$ and a 16-bit 3rd order sigma delta modulator. A highly selective band-pass filter is implemented into the digital domain, incorporated in the decimator block of the sigma-delta converter; in this way it is possible to reduce total area (which is $0.4mm^2$ for a single input channel) and power consumption ($250\mu W$, single channel) in the integrated, implantable module. Simulation results prove the capability of the proposed system to record signals whose magnitude is in the order of tens of microvolts thanks to the low Input Referred Noise (IRN) of $2.4\mu V_{rms}$ of the input stage.

1 INTRODUCTION

In the last decades, research on biomedical engineering has been widely propelled by many groups with the aim to find a solution for a number of diseases and to grant a better quality of life to patients. One of the topics that has been subject to a great attention is the interface between the human nervous system and the machines (BMI). Such studies have a wide range of potential applications: from diseases affecting the nervous systems (like Parkinson, epilepsy, multiple sclerosis) to treatment of permanent damages of the spinal cord and, finally, prosthetics (Pereira et al., 2007; Liu et al., 2000; Von Arx and Najafi, 1999). This work is included in the latter field: our aim, in fact, is to develop a system capable to record the signals captured by an electrode inserted in the peripheral nervous system of an amputee patient and exploit them to drive a robotic limb. With this approach, there are several advantages with respect to the more traditional Electromyographic (EMG) prostheses. First, the limb will be controlled using the thought, thus allowing the patient to feel the prosthetic arm as a natural extension of his/her body. Secondly, the insertion of the electrode inside the nerves makes it possible to restore the sensory feedback, providing current pulses whose shape, frequency and amplitude can be programmed according to stimuli coming by temperature and pressure sensors collocated on the robotic limb (Micera et al., 2010; Dhillon and Horch, 2005). The main problem, in this kind of application, is the weak amplitude of the extracellular nervous signals that can span in a range from few microvolts to 500 microvolts (Harrison and Charles, 2003; Yoshida and Stein, 1999; Loi et al., 2011). Moreover, such signals are drowned in a noisy environment mainly due to electromyographic (EMG) interferences from the muscle fascicles surrounding the nerves; EMG signals are in the order of magnitude of millivolts, thus several times the amplitude of the neural signals. Furthermore, power spectral densities (PSD) of the interferences and of the useful signal are very close and partially overlap (Rieger et al., 2003; Harrison, 2007). In this context, it is mandatory to properly amplify the weak useful signal and to filter out the huge noise component. Given the partial overlap of the PSDs, a highly selective filter is needed to reject most of the interferences. The implementation of such a circuit in the analog domain is possible and it is a widely used approach (Guo et al., 2004; Lee and Lee, 2005; Limnuson et al., 2009), but it implies a number of problems in the design: highly selective filters are prone to instability and cascading many amplifiers is power consuming. Such problems make the implementation of an integrated device for chronicle implants difficult. In our approach, we propose to adopt a sigma-delta architecture which is capable to shift most of the complexity of the realization either of the highly se-

Carboni C., Loi D. and Barbaro M..
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DOI: 10.5220/0003782802070212
In *Proceedings of the International Conference on Biomedical Electronics and Devices* (BIODEVICES-2012), pages 207-212
ISBN: 978-989-8425-91-1

lective filter and of the analog-to-digital conversion in the digital domain thus keeping only a small analog circuitry in the implantable chip. In this way a more robust and noise immune system can be designed with a lower power consumption. The device is therefore made up of two modules: an implantable integrated circuit and an external board. The microchip hosts only a first-order pre-amplifier/pre-filtering stage and the sigma delta modulator (each of which for every input channel) while the highly selective filter is implemented altogether with the decimator on the external digital platform. In this paper we present the design and the simulation results concerning the analog part of the recording path. In section 2 we present the architecture of the whole system, while in sections 3 and 4 we report the design choices respectively for the pre-amplifier/pre-filtering block and for the delta-sigma modulator. Simulation results are provided in section 5.1 and conclusions are drawn in section 6.

2 SYSTEM ARCHITECTURE

The block diagram in Fig. 1 shows the system architecture which is composed by two main blocks: the analog front/end and the digital processing unit. The analog module was designed in a 0.35μm CMOS process from AMS (Austriamicrosystems) with double-poly capacitors, 3.3V power supply and 4 metal layers. Area and power constraints are particularly compelling since the chip must be integrated with the electrode and implanted in the patient stump. The front-end module works in a bidirectional way, it implements basic signal conditioning on the incoming neural signal (in recording mode) and provides current pulses on the feedback path (in stimulation mode). The signal is, thus, filtered and amplified by the Pre-Filtering/Pre-amplifier block as close as possible to the recording site. In this way, the noise due to long cables and connection paths can be avoided. The conditioned signal is then converted into a 1-bit digital stream by the delta-sigma modulator and sent to the digital module for decimation and further processing. One of such signal's streams is needed for each input channel if the device is connected to a multichannel electrode. The digital module is hosted on an external board; it implements the decimation block of the sigma-delta converter altogether with the highly selective bandpass filter. The digital module is also responsible of the generation of digital programmable stimulation waveforms and of management of the communication between the artificial limb and the electrodes. The digital unit will be implemented on programmable logic (FPGA), hosted on the robotic limb. A further advantage of such approach, is the possibility of changing the selectivity of the filter on the fly by adjusting the digital parameters.

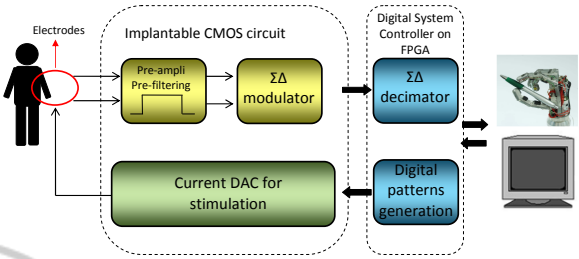


Figure 1: Block diagram of the recording and stimulation system.

3 PRE-AMPLIFIER AND PRE-FILTERING

Fig. 2 shows the pre-amplifier/pre-filtering block that was implemented with a first order switched capacitor (SC) filter. SC-filters have, in fact, the great advantage, over their continuous-time counterpart, to achieve a better precision in the cut-off frequency implementation. The Bandpass Filter (BPF) was realized cascading a Highpass filter (HPF) with a Low-pass Filter (LPF); the HPF is used as first stage in order to start rejecting the EMG interferences as close as possible to the electrode, before any amplification. The filter specifications required a bandwidth between 800Hz and 8kHz and a gain of 200V/V. This gain value has been determined to maximize the amplification at neural frequencies avoiding the risk of amplifier saturation. In Table 1 the values used for the filter capacitance are summarized.

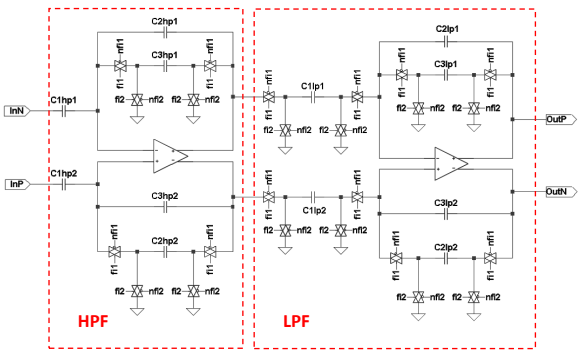


Figure 2: Band-Pass filter.

The switches were realized using transmission gates at minimum size in order to reduce area. A

Table 1: Filter Capacitance values.

C	Value [pF]	C	Value [pF]
$C_{1hp1,2}$	80	$C_{1lp1,2}$	10
$C_{2hp1,2}$	13	$C_{2lp1,2}$	1.6
$C_{3hp1,2}$	1.7	$C_{3lp1,2}$	2

simple cascode symmetrical OTA (Fig. 3) was chosen for the operational amplifier implementation and it was carefully dimensioned in order to minimize the Input Referred Noise (IRN). Flicker noise is one of the major concerns, given the low frequencies of the neural signal, thus a p-type differential pair with large area was adopted to minimize this contribute (Razavi, 2001). Thermal noise was addressed using a large g_m for the differential pair and reducing the g_m of the output branch transistor (Harrison and Charles, 2003) according to the formula:

$$v_{n,th} = \frac{16kT}{3g_{m1}}\left(1+\frac{g_{m6}}{g_{m1}}+\frac{g_{m12}}{g_{m1}}\right)$$

where k is the Boltzmann constant, T the absolute temperature and g_{mx} the transconductance of transistor x. In Table 2 all sizes are reported, all transistors were biased with a $4\mu A$ current. A passive SC common mode feedback block was used for power saving.

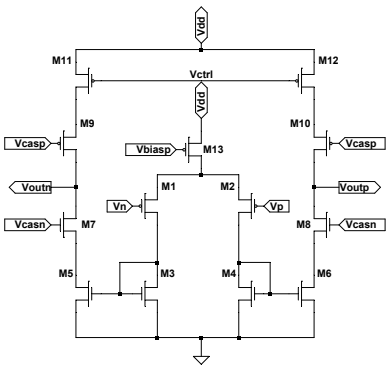


Figure 3: Symmetrical OTA.

Table 2: OTA dimensions.

	$\frac{W}{L}[\frac{\mu m}{\mu m}]$		$\frac{W}{L}[\frac{\mu m}{\mu m}]$
$M_{1,2}$	$\frac{800}{10}$	$M_{7,8}$	$\frac{15}{20}$
$M_{3,4}$	$\frac{5}{20}$	$M_{9,10}$	$\frac{15}{20}$
$M_{5,6}$	$\frac{5}{20}$	$M_{11,12}$	$\frac{5}{20}$

4 SIGMA-DELTA MODULATOR

Once that the useful signal has been properly amplified it is possible to convert it in the digital domain. With this purpose, a third order switched capacitor sigma-delta modulator in a Cascade of Integrators with FeedBack (CIFB) configuration was designed. The weakness of the neural signals required to adopt a 16-bit converter; with a reference voltage of $V_{ref} = 2V_{pp}$, a $LSB = 0.15\mu V$ can be achieved, allowing the detection of microvolt level signals. This result was achieved using an $OSR = 128$ with a sampling frequency $f_s = 2.048MHz$. Due to long simulation time, preliminary tests were performed using a behavioral model in Simulink environment and, only once that the specifications were satisfied, the circuit was implemented at transistor level.

4.1 Behavioural Simulink Model

A Simulink model has great advantages in terms of simulation time saving moreover, it allows the introduction of blocks modelling noise sources and opamp non-idealities thus granting an excellent reliability of the system and a good agreement with transistor level simulations. Fig. 4 shows the diagram block used for this purpose.

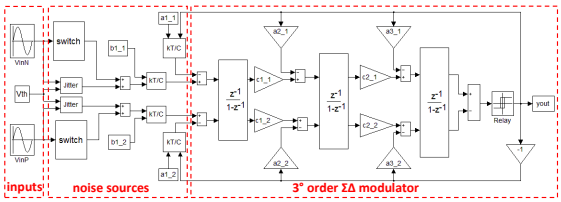


Figure 4: Sigma-delta modulator: behavioural Simulink model.

The model is a modification of what presented in (Malcovati et al., 2003) and (Zare-Hoseini et al., 2005) which take into consideration saturation, slew rate, finite gain and bandwidth limitations. KT/C noise, thermal noise of the amplifier, switches non-idealities and clock jitter effects have also been included. With respect to the original model our system was transformed in a fully differential architecture in order to make it more similar to the actual transistor implementation (shown in the following subsection). The coefficients (summarized in in Table 3) were chosen using the Schreier Toolbox (Schreier and Gabor C., 2001) with a 18-bits target resolution (we added 2 bits for noise margin).

The mismatch effects were also taken into consideration since the coefficients have been generated

Table 3: Sigma delta modulator: coefficients.

Coefficient	Value	Coefficient	Value
a_1	0.05	b_1	0.05
a_2	0.3	c_1	1
a_3	0.8	c_2	1

as capacitor ratios, whose values have been extracted randomly from a normal distribution within a 6σ range around the nominal value.

4.2 Transistor Level Design

The block diagram described in the previous section was mapped into a transistor level design using a SC circuit. The main components are the discrete time integrators shown in Fig. 5 (first stage) and Fig. 6 (second and third stages). It can be observed that all the feedback paths have been realized driving a switch with the quantizer output and connecting the corresponding capacitor to the reference voltages $V_{ref-} = V_{dd}/2 - 1$ and $V_{ref+} = V_{dd}/2 + 1$. Since the a and b coefficients are equals, in the first stage the same capacitor was shared for the two paths while in the second and third stage two different capacitors were used in order to implement coefficients a and c.

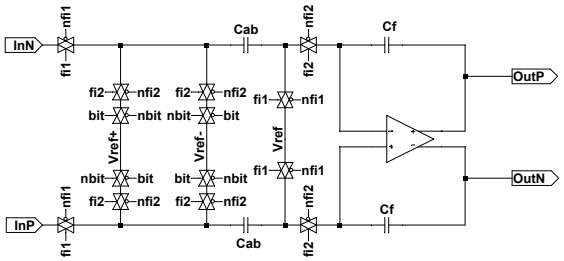


Figure 5: Sigma-delta modulator: first integrator schematic.

In Table 4 all the values used for the capacitors are reported, each coefficient can be obtained by capacitance ratios using the relationship $x = C_x/C_f$. A simple symmetrical OTA was used to realize the operational amplifier, it has been sized in order to meet the specifications determined with the behavioral simulation (in terms of DC gain, GBW, dynamic range and slew rate). The single bit quantizer has been designed with a track and latch circuit.

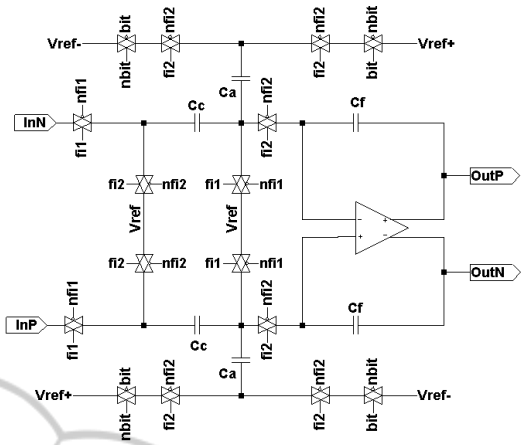


Figure 6: Sigma-delta modulator: second and third integrator schematic.

Table 4: Sigma-Delta modulator: capacitance values.

C	Value [pF]	C	Value [pF]
$C_{ab,1st}$	0.2	$C_{f,2st}$	4
$C_{f,1st}$	4	$C_{a,3st}$	3.2
$C_{a,2st}$	1.2	$C_{c,3st}$	4
$C_{c,2st}$	4	$C_{f,3st}$	4

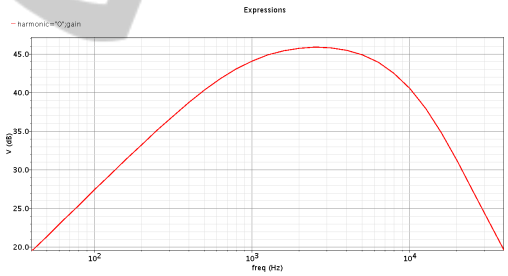


Figure 7: Bandpass filter: Frequency response.

5 SIMULATION RESULTS

5.1 Pre-amplifier/Pre-filter Results

The frequency response of the operational amplifier of Fig. 3 shows a DC-gain of $108dB$ with a $GBW = 1MHz$, the 62^o phase margin ensures a good compromise between ringing avoidance and settling time. The integrated input referred noise in the bandwidth $800Hz - 8kHz$ is $2.1\mu V_{rms}$ allowing to detect signals in the order of magnitude of tens of microvolts. The bandpass filter provides a gain of $46dB$ within the $3dB$ bandwidth $800Hz - 7.2kHz$ (Fig. 7) and the simulated noise in this bandwidth is $2.4\mu V_{rms}$. The gain

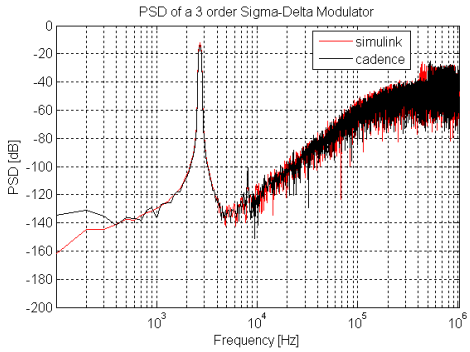


Figure 8: Sigma-Delta modulator PSD: behavioral simulation (red curve) and transistor level simulation (black curve).

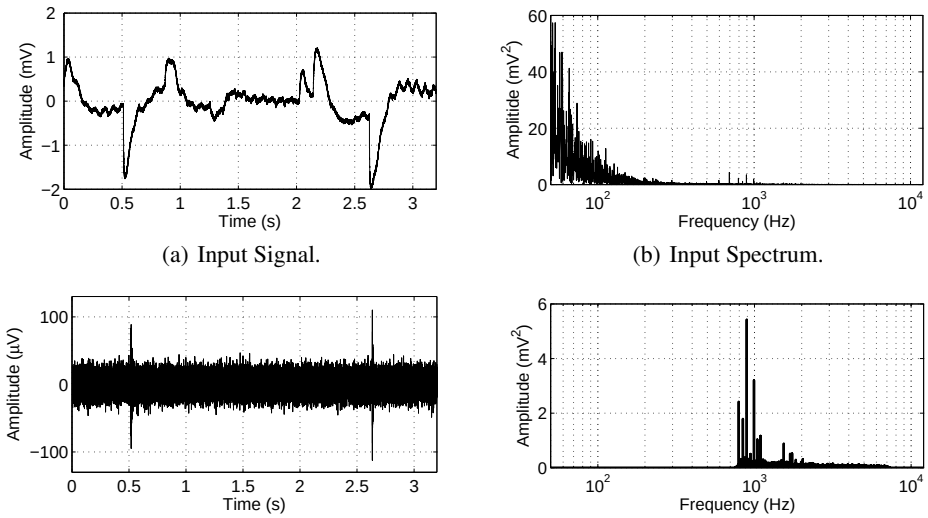
value was chosen to avoid the risk of saturation due to EMG interferences. We considered a worst condition of a $10mV$ interference at $300Hz$. In this case, the gain at $300Hz$ is $65V/V$ thus the residual EMG signal at the output of the filter will be $650mV_{pp}$, far away to rich the saturation limit of $2V_{pp}$ of the sigma-delta modulator. This residual out of band huge interference will be completely rejected in the digital domain by the high-selective band pass decimator.

5.2 Sigma-delta Modulator Results

The power spectral density (PSD) of the sigma-delta modulator, is shown in Fig. 8: the red curve represents the results obtained by Simulink simulations while the black one is the PSD extracted by the transistor level simulation performed with Cadence. As it can be observed, the two curves are very similar each other, confirming the good agreement between the two models. The final resolution achieved is $16.12bit$ corresponding to a $SNR = 98.8dB$ with an $OSR = 128$. The system functionalities have been tested using, as modulator input, pre-recorded neural patterns, on the basis of recordings made in clinical trials with rabbits. The input pattern, represented in Fig. 9(a), corresponds to 3.2 seconds of recording during which the rabbit was subjected to vibrations at 50Hz and 100Hz in cutaneous afferents. The input signal is affected by EMG and ECG interferences with a very large amplitude (in the millivolts range) and a spectrum (Fig. 9(b)) concentrated below 300Hz. Such interferences completely mask the underlying neural content. The signal has been processed by the delta-sigma modulator and then decimated and band-pass filtered using a digital filter in simulink environment. Fig. 9(c) displays the input-referred output signal and Fig. 9(d) its power spectral density: the low-frequency interferences are completely removed and the weak neural signal (in the microvolts range) is now visible, as well as its frequency signature. In Table 5 the main characteristics of the system are summarized.

6 CONCLUSIONS

A bio-electronic interface for peripheral neural signal recording was designed. The first stage is composed by a first order pre-amplifier and pre-filtering block



(a) Input Signal. (b) Input Spectrum.

(c) Output Signal. (d) Output Spectrum.

Figure 9: Sigma Delta modulator: pre-recorded neural signal processing.

Table 5: Main parameters summary. Data are referred to each input channel.

parameter	value
Gain	$46dB$
f_L, f_H	$800Hz, 7.2kHz$
Power	$250\mu W$
Area	$0.4mm^2$
IRN	$2.4\mu V_{rms}$
resolution	$16.12bit$

that provides a gain of $200V/V$ in the bandwidth range $800HZ - 7.2kHz$. The signal is then converted in the digital domain by a 16-bit sigma delta modulator and transmitted to the digital part of the system for decimation, highly selective band-pass filtering and further signal processing. The analog front-end of the designed system (prefiltering/preamplifier and sigma-delta modulator) exhibits a total area of $0.4mm^2$ with a $240\mu V$ power consumption (for each input channel). Simulation results show that the system is capable to record a neural signal in the order of magnitude of tens of microvolts thanks to its low IRN equal to $2.4\mu V_{rms}$.

ACKNOWLEDGEMENTS

The work described was supported by MIUR (Italian Ministry of Education, University and Research) through project Openhand (PRIN 2008). The authors wish to thank Laura Muggianu for helping with the design and simulations and Silvestro Micera of Scuola Superiore Sant'Anna di Pisa (SSSA) for neural traces providing.

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