

Design of Pulse Power Supply Voltage Acquisition and Adjustment System Based on AD7888

Qing Wang, Yongbin Zhang, Jinming Chen, Guangmin Liu and Feng Wang

*Institute of Mechanical Manufacturing Technology, China Academy of Engineering Physics, Mianyang, Sichuan, China
chenjmcaep@sina.com*

Keywords: Pulse power supply, AD7888, SPI bus, Voltage acquisition, Voltage feedback adjustment.

Abstract: The precision of the output current of the pulse power applied to precision electroplating is an important factor that affects the quality of the plating. To accurately control the current requires precision acquisition of the power voltage in real-time. This paper introduces the hardware interface and the implementation procedures of the voltage acquisition module in detail. In the voltage acquisition module, FPGA is the main controller and the AD7888 is an analog to digital converter (ADC). They are linked by the SPI bus. The program is based on the timing of AD7888 interface. It can realize the SPI bus serial communication between FPGA and AD7888 and take up fewer resources. Based on the real-time acquisition voltage of AD7888, we choose the proper duty cycle step size in different voltage intervals by fitting the power characteristic curve, so as to achieve fast and accurate adjustment of the pulse power supply voltage.

1 INTRODUCTION

Electroplating is a technique commonly used to improve the appearance and surface properties of the workpiece. Pulse electroplating can obviously improve the quality of the coating by using pulse current. Pulse electroplating power is a device to produce pulse waveform, and the stability of its output current is an important factor that affecting the quality of the electroplating layer. In general, the current is precisely controlled by monitoring the current value in real-time. During the commissioning of the pulse power supply, the voltage at both ends of capacitor is used as reference voltage, and the voltage's stability is much higher than that of current. By collecting voltage value in real time, the error of data acquisition can be reduced obviously. When the circuit components are determined, there is a fixed function relationship between the voltage and the current. Therefore, in this paper, a suitable ADC is selected and the SPI bus is utilized to connect the ADC with the main controller to realize the real-time acquisition of voltage equivalent. Collected voltage equivalent data are used as the reference value of the control voltage, and the reference value of the voltage is compared with the set value, and the precise control of voltage can be realized through closed loop feedback adjustment.

2 INTERFACE DESIGN BETWEEN FPGA AND AD7888

2.1 System Construction

The system structure is given in Figure 1. The field programmable gate array (FPGA) is configured flexibly and is used as the main controller. Functional modules in FPGA include voltage sampling processing unit, forward pulse control unit and voltage adjustment unit. In the voltage sampling processing unit, the real-time monitoring of the voltage is realized by the ADC. The selection of AD Chips should take the speed, precision, power, cost and installation of the system into account. AD7888 is a 12 bit 8 channels ADC with the minimum and the lowest power consumption. The voltage adjustment in the voltage regulating unit is realized by controlling the MOSFET Q_1 on and off. The forward pulse control unit is used to generate the forward pulse waveform, changing the break time of Q_2 can output pulse waveform with different duty cycle.

AD7888's pin configurations are illustrated in Figure 2. AD7888 uses a single power supply, working from 2.7V to 5.25V, and its maximum pass rate is 125kSPS.

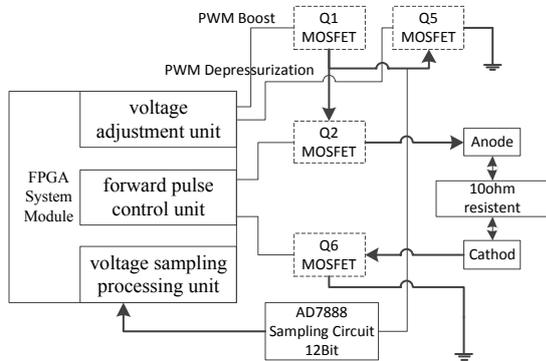


Figure 1: The system structure.

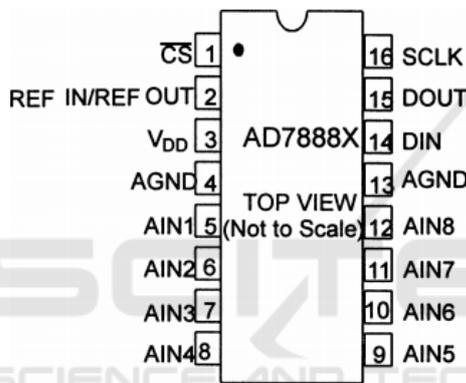


Figure 2: AD7888's pin configurations.

Its control words are introduced from the DIN pin to the 8-bit, only written control register on the rising edge of the control clock (CLK). The serial interface timing diagram of AD7888 is illustrated in Figure 3. The completion of a digital conversion requires 16 serial clock cycles, in which the control word is input to the control register on the rising edge of the first 8 clock pulses. The converted data are output bit by bit by the DOUT pin while the conversion results are read out. When using the chip, the chip select signal should be at least 10 ns earlier than the falling edge of SCLK, serial data after the analog-digital conversion should be output by DOUT within 100ns.

The SPI bus is a serial interface commonly used in AD7888, which has the characteristics of little connection and good independence. A typical SPI bus consists of a serial clock line (SCLK), a master output / slave input line (MISO) and a master input / slave output line (MISO) and a slave select line (SS). All of the data transfers are synchronized with the serial

clock, and the transmission of 1Bit data requires a clock pulse.

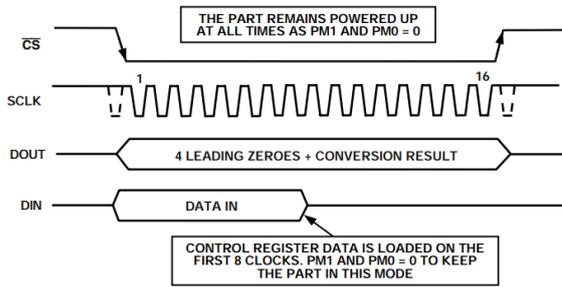


Figure 3: Serial Interface Timing Diagram of AD7888.

The control time series of SPI bus can be realized by FPGA through Verilog language programming.

The standard SPI bus IP core occupies more on-chip resources. This design uses a simple method to simulate the analog SPI interface between FPGA and AD7888 by programming.

2.2 FPGA and AD7888 Verilog Interface Description

In order to guarantee the normal operation of AD7888, a periodic square wave should be input as a chip select signal at the / CS pin. The control clock is input from the CLK pin. The control word is written into the control register within AD7888 through DIN. The AD converted 12-bit data are output from DOUT to the FPGA's internal registers. According to the above requirements, the SPI bus interface module consists of four parts, including the clock generation module, the data input register, the control state machine and the shift register. The clock generation module divides the 50 MHz clock provided in the system to get the working clock CLK of the AD7888. The control register's reference clock is CLK. The control state machine controls the shift operation of the input / output shift register and generates the chip select signal / CS. The data in the input shift register is output by DIN. Data output via DOUT is stored in the output register through the output shift register. They combine into a complete 12-bit data. Figure 4 is the interface structure between the SPI bus and AD7888.

The interface program is based on the working sequence and principle of the AD7888. The working clock of AD7888 should take into account the number of acquisitions of voltage value and the speed of acquisition. AD7888 work at full power and uses internal benchmarks to collect data from the AIN1 channel. According to the above setting, the control word put

into AD7888 is 8'b0. The program flow chart is given in Figure 5. Figure 6 is an interface module that is compiled by the program.

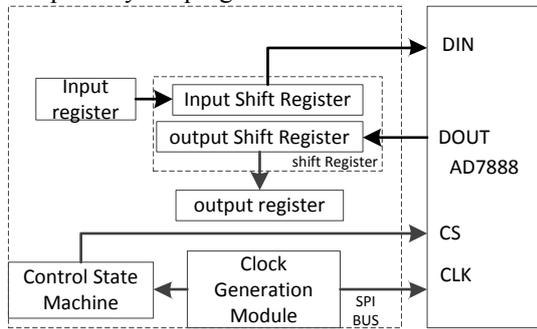


Figure 4: The interface structure between SPI bus and AD7888.

When starting to collect the voltage value, the chip select signal of AD7888 changes from high level to low level.

```
parameter[7:0]Control_Register=8'b0;
//DOONTC/ZERO/ADD2/ADD1/ADD0/REF/PM1/PM2
always@(posedge clk1M)
begin
    case(cnt2)
        17'd0 : begin
            ad_cs_n <= 1'b1;
            ad_clk <= 1'b1;
            ad_din <= 1'b0;
            adc_temp_data <= 12'b0;
            end
        17'd1 : begin
            ad_cs_n <= 1'b0; //start
            ad_clk <= 1'b1;
            ad_din <= 1'b0;
            end
        17'd2 : begin
            ad_cs_n <= 1'b0;
            ad_clk <= 1'b0;
            ad_din <= Control_Register[7];
            //write Control_Register
            end
        17'd3 : begin
            ad_cs_n <= 1'b0;
            ad_clk <= 1'b1;
            // the first rising_edge clk
            ad_din <= Control_Register[7];
            end
    endcase
end
```

Other control words are written to the control register in the same way from high to low.

```
17'd10 : begin
    ad_cs_n <= 1'b0;
    ad_clk <= 1'b0;
    ad_din <= Control_Register[3];
end
17'd11 : begin
```

```
    ad_cs_n <= 1'b0;
    ad_clk <= 1'b1;
    //5 rising_edge clk
    ad_din <= Control_Register[3];
    adc_temp_data[11] <= ad_dout;
end
17'd12 : begin
    ad_cs_n <= 1'b0;
    ad_clk <= 1'b0;
    ad_din <= Control_Register[2];
    adc_temp_data <= adc_temp_data;
end
17'd13 : begin
    ad_cs_n <= 1'b0;
    ad_clk <= 1'b1;
    //6 rising_edge clk
    ad_din <= Control_Register[2];
    adc_temp_data[10] <= ad_dout;
end
```

The data after the analog digital conversion is output at the rising edge of each synchronous clock and is locked at the drop edge of the clock.

```
17'd33 : begin
    ad_cs_n <= 1'b0;
    ad_clk <= 1'b1;
    //16 rising_edge clk
    adc_temp_data[0] <= ad_dout;
end
    After completing a data acquisition, the chip select signal is set to high.
17'd34 : begin
    ad_cs_n <= 1'b1;
    ad_clk <= 1'b1; //over
    adc_temp_data <= adc_temp_data;
    adc_data_r <= adc_data_r + adc_temp_data;
    if(cnt3 == 5'd29)
    begin
        adc_data <= adc_data_r / 30;
        adc_data_r <= 16'b0;
    end
    else
        adc_data <= adc_data;
    end
end
```

Define a counter to count the data collected by AD7888. If the value of the counter reaches 29, the current accumulative value is divided by 30 to get the average value of the voltage. Utilizing the above treatment can significantly reduce the voltage acquisition error.

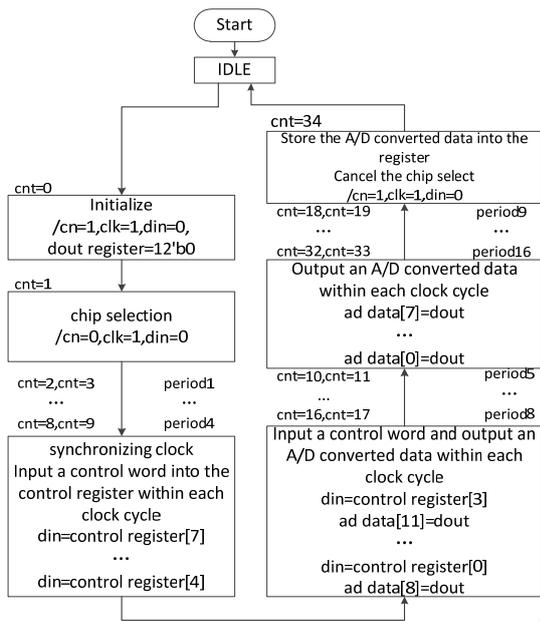


Figure 5: The program flow chart.

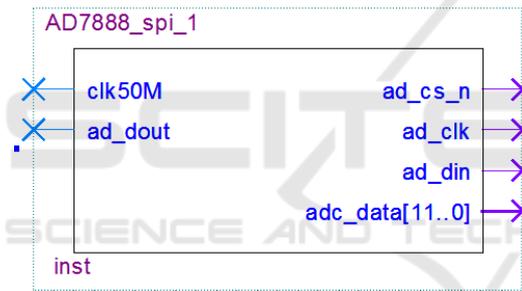


Figure 6: AD7888-SPI interface module.

2.3 Simulation and Verification

When the occupied space is relatively small, the data of AD7888 is collected by signaltap. Otherwise, use the serial port assistant to collect the voltage signal. Signaltap can capture and display real-time signals. In Figure 7, both real-time data and average data over 30 acquisitions acquired from AD7888 can be observed. Serial port assistant can receive the binary data that FPGA outputs after connecting with FPGA through RS-232. The results are shown in Figure 8. The duty cycle of Q1 is set to 7500 and the voltage equivalent value of the AD7888 is converted to 107 or 108 in decimal.

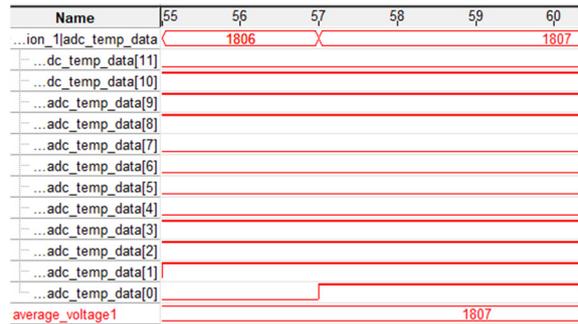


Figure 7: Real-time data and average data required from AD7888.

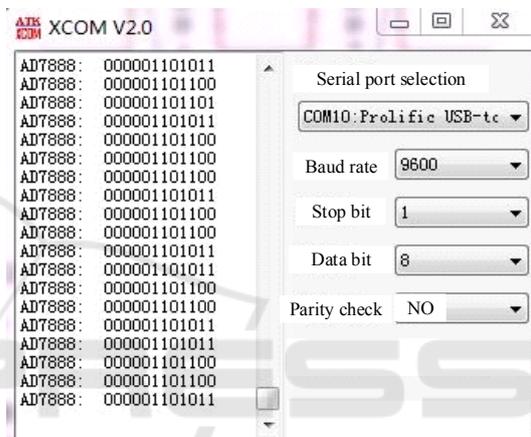


Figure 8: The serial port assistant required binary data from AD7888.

Signaltap and Serial Assistant show the AD7888 analog to digital conversion of the average voltage value, and the design of the circuit voltage is expected, the functional simulation results are correct.

3 VOLTAGE ADJUSTMENT MODULE DESIGN

The main function of the voltage adjustment module is to make the pulse power supply accurately and quickly output the target voltage. Figure 9 shows the power supply voltage adjustment and measurement principle. The voltage across capacitor P₂ can be modified by adjusting the duty cycle of MOSFET Q₁. The cycle / pulse width is used to represent the duty cycle in this article's programming and experimentation. In the power test stage, when Q₁'s duty cycle x is constant, the actual voltage V_{act} of the capacitor P₂ can be measured by a multimeter, and the voltage equivalent V_{equ} at the current duty cycle x can be

monitored using the AD7888. Based on the above measurements, two functional relationships between the V_{equ} and V_{act} , x and V_{act} can be established. Based on these two functional relationships, the voltage across P_2 can be adjusted to the error of the set voltage by adjusting the duty cycle of Q_1 .

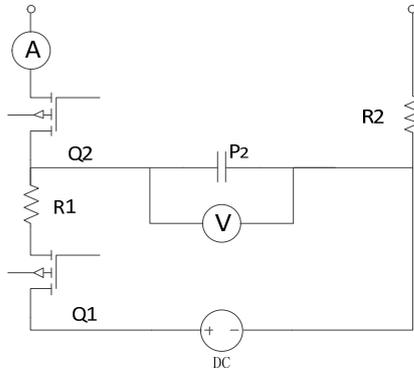


Figure 9: the power supply voltage adjustment and measurement principle.

3.1 Pulse Power Experiment and Data Processing

In the pulse power experiment, the pulse width of the output pulse waveform is $50 \mu s$ and the duty cycle is 10. The pulse width of Q_1 is $1 \mu s$, and its duty ratio varies between 1~10000. Some of the experimental data are given in Table 1. The obtained experimental data are fitted with origin for function fitting. The point corresponding to the voltage equivalent V_{equ} and the actual voltage V_{act} value are depicted in the coordinate system. It can be observed that the functional relations between them are approximately linear and have insignificant inflection points. Therefore, linear and piecewise linear fitting function relations are chosen respectively. The formula of function relation obtained by linear fitting is

$$y = a + b * x \tag{1}$$

The formula of function relation obtained by piecewise linear fitting is

$$x < x_i, y = a_1 + k_1 * x \tag{2}$$

$$x > x_i, y = a_2 + k_2 * x \tag{3}$$

The results obtained are shown in Figure 10. The difference between the fitting value and the actual value obtained by the two fitting methods is shown in Figure 11.

In Figure 10, the fitting result of (a) is

$$y = -94.995 + 3.364x \tag{4}$$

The fitting result of (b) is

$$y = -1468.854 + 4.192x \tag{5}$$

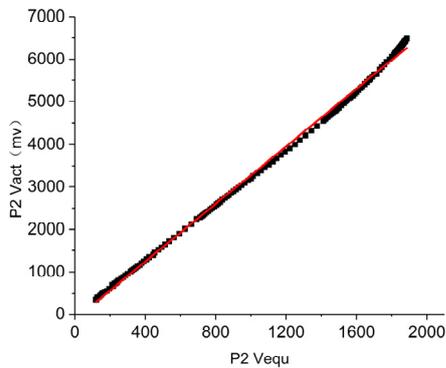
Table 1 Experimental data

Serial Number	Duty cycle Q1	V_{equ}	P2 V_{act} (mv)
1	1	1886	6480
2	5	1867	6380
3	15	1837	6230
4	25	1801	6060
5	35	1771	5940
6	40	1759	5870
7	35	1771	5940
8	75	1673	5510
9	100	1611	5270
10	135	1538	5000
11	170	1465	4750
12	300	1251	4000
13	400	1126	3600
14	520	1001	3200
15	680	875	2800
16	840	780	2500
17	2000	446	1400
18	2900	326	1040
19	5000	212	698
20	9000	127	408

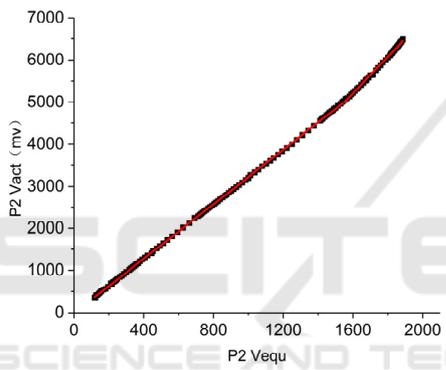
The function is segmented when the V_{equ} of P_2 is 1507. Figure 11 shows the difference between fitted values obtained by two methods and actual values. The fitted values obtained by the piecewise linear fitting method is far less than those obtained by the linear fitting method. Therefore, piecewise linear fitting is applied to the voltage adjustment module. In the experiment, the pulse width of Q_1 , Q_2 and the Q_2 duty cycle remain unchanged, Q_1 's duty cycle changes from 1~10000, the voltage equivalent value collected by AD7888 can be converted to the actual voltage value by this function relation. Figure 12 shows the fitting results between Q_1 's duty cycle and V_{act} .

$$y = 10^5 / (15.783 + 0.0295x) \tag{6}$$

The function relation between them is approximately inverse proportionate.



(a)



(b)

Figure 10 (a)Linear Fitting of Experimental Data
(b)Piecewise Linear Fitting of Experimental Data

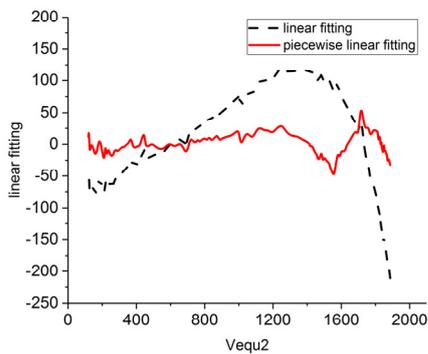


Figure 11: The difference between the fitting value and the actual value by the two fitting methods.

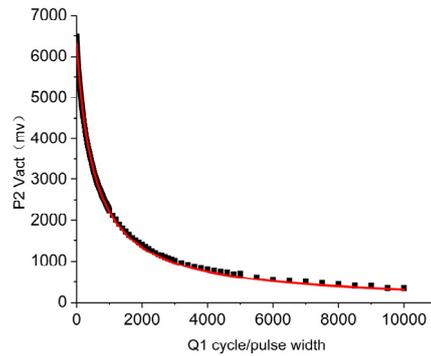


Figure 12: The fitting results between Q1's duty cycle and Vact.

3.2 The Principle of Voltage Adjustment and Its Verilog Implementation

Voltage adjustment is based on feedback adjustment. The method of voltage adjustment is to select the suitable duty cycle step length in different voltage intervals. When the setting voltage is V_{set} , the principle of voltage adjustment is based on the functional relationship between V_{equ} and V_{act} , and the functional relationship between x (the duty cycle of Q_1) and V_{act} . To make the power supply output to the set voltage, firstly, an approximate value x_0 of x is determined as an initial value by the function of the x and V_{act} (The error of this function is larger). x changes in certain steps, at the same time, use the AD7888 to monitor the voltage obtained at the corresponding value of x . Secondly, convert V_{equ} into V_{act} through the functional relationship between V_{equ} and V_{act} . Thirdly, compare V_{act} with V_{set} . When $|V_{act} - V_{set}| < 20mV$, keeps the value of x unchanged and output the voltage corresponding to x .

Based on the above principle, the voltage adjustment process is optimized to enable the power supply to output the set voltage accurately and quickly. Obviously, the function between x and V_{act} is similar to the inverse proportion. In the range of $V_{act} > 6V$, to prevent the occurrence of $x < 0$ in the calculation, the interval above 6V in this functional relationship is approximately treated as a linear relationship. The function relations in other intervals remain unchanged. In order to obtain the initial duty cycle x_0 closer to the exact value. From the function relation of x and V_{act} , when V_{act} is greater than 5V, V_{act} varies by more than 30mV each time the value of x is changed by 1. If the step length of x is kept at 1, this will make the voltage fail to reach the set value. If the step length of x is too small, the voltage adjustment process will be slow. Therefore, different steps are selected in different

range of x values to meet the needs of the power supply for accurate and rapid voltage adjustment. Voltage adjustment flow is shown in Figure 13.

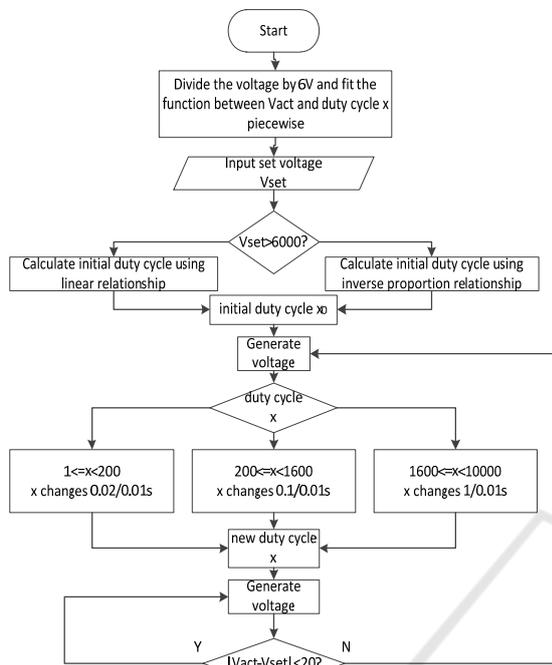
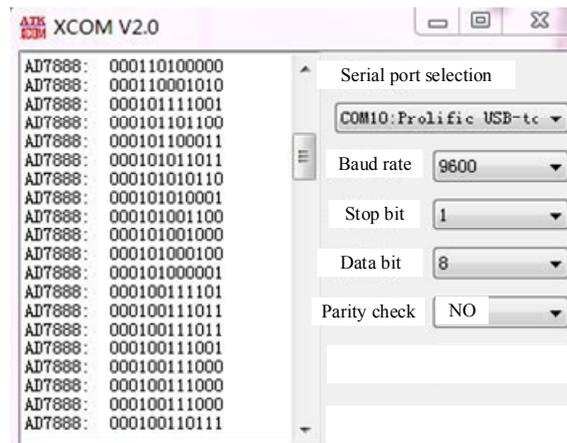


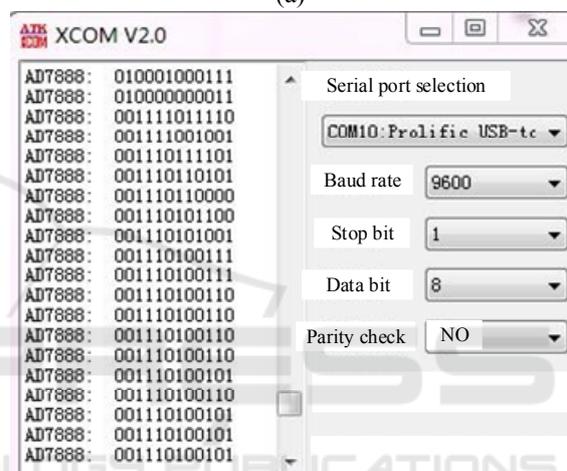
Figure 13: The voltage adjustment flow.

3.3 Experimental Result

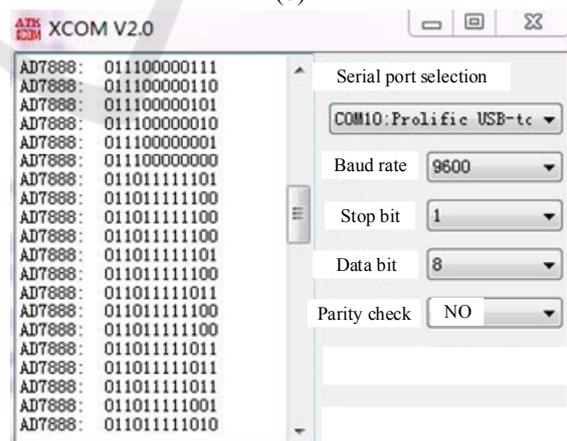
In the voltage adjustment experiment, the voltage values are set to 1V, 3V and 6V, respectively. Using a serial port assistant to receive real-time voltage equivalent values in the voltage adjustment process collected by AD7888. The results are given in Figure 14. When the data is received at the 9600 baud rate, the voltage equivalent value can be stabilized within 15 sets of data. Therefore, when the error range of voltage adjustment is set within 30mV, the voltage adjustment module can be used to output an accurate and stable voltage within 10s.



(a)



(b)



(c)

Figure 14: Voltage adjustment results received by serial port assistant. (a)Vset is 1V, (b)Vset is 3V, (c)Vset is 6V.

4 CONCLUSIONS

This paper introduces a kind of SPI bus interface design, which takes the FPGA as the main controller, the AD7888 as the ADC. The serial communication between FPGA and AD7888 is realized by programming. Real-time voltage monitoring data for pulse electroplating power supply can be obtained by signal tap or serial port assistant. The program occupies less FPGA on-chip resources. On the basis of real-time monitoring of supply voltage, the method of adjusting the voltage is Choose different duty cycle steps in different voltage intervals. The voltage is set to approach the set voltage by calculating the initial duty cycle. The duty cycle value is then changed by closed-loop feedback. This causes the pulse power supply to output the desired voltage. The experimental results show that the voltage equivalent value collected by AD7888 is in accordance with the actual voltage. The voltage adjustment is accurate and fast, it meets the requirements of the use of pulse power supply, and the reliability is high.

ACKNOWLEDGEMENTS

The authors appreciate the support from the National Natural Science Foundation of China (Grant No. 51475439) and Sichuan Provincial Science and Technology Department of application-based projects (Grant No. 2016JY0109).

REFERENCES

- [J]. Chinese Journal of Nuclear Electronics and Detection, 2014,34 (05): 598-601.
- Zhen Wang, Ludan Li. *Design of Airborne 270V DC Monitoring System Based on AD7888 Chip* [J]. Information Systems Engineering, 2017 (09): 126-127 + 129.
- Kewang Zheng, Daibo Xing, Tenguan Ding. *Design of voltage acquisition module based on FPGA in network acquisition system* [J]. China Science and Technology Information, 2017, (10): 75-77.
- Gang JIN, Zhong CHEN, Yue HONG. *Application of Synchronous Serial SPI in AD7888 and AT90S8515 Interface* [J]. Microcomputer Information, 2004, (02): 91-92.
- Jian-ze WANG, Yu-ming PEI, Jia YANG. *Application of Analog to Digital Converter AD7888* [J]. Journal of Jilin University of Architecture & Civil Engineering, 2010, 27 (4): 53-56.
- Tao Geng, Guochao Li, Bingqiang Li, Ying Gao. *Design and Implementation of Analog-to-Digital Converter AD7888 Interface Based on FPGA* [J]. Journal of Information and Computers (Theory Version), 2014 (04): 31-33.
- Chunqing Xuan. *Design and implementation of embedded portable measuring instrument based on AD7888*