Power Quality Monitoring Device of EMU Traction Network Based on Zynq

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Keywords: EMU, Power Quality, Monitoring Devices, Zynq-7000, AD9251.

Abstract: Aiming at the power quality problem of traction network during the operation of moving train sets, a traction network power quality monitoring device is designed in the paper. The device uses the XC7Z045 chip of the Zynq-7000 series as the main control chip, and adopts a modularized design, including the signal acquisition module, signal processing module, data transmission module and power supply module. The signal acquisition module designs a 1000:1 large-ratio resistor-capacitor buck circuit and a current sampling circuit with a gain of 3.9, and realizes the high-speed synchronous acquisition of network voltage and network current based on the AD9251 chip; the signal processing module completes the high-speed processing of data by using the built-in FPGA+ARM dual-core architecture of the main control chip; the data transmission module uses the Ethernet chip 88E1116R and network transformer HR682430E to construct the PAC and the data transmission module; the signal processing module uses the Zynq-7000 series XC7Z045 chip as the main control chip. The data transmission module uses Ethernet chip 88E1116R and network transformer HR682430E to build PHY Gigabit network circuit, which realizes high-speed and reliable data transmission; the power supply module is based on a variety of power management chips such as TPS54560, SY8263, and so on, and the logic of power supply architecture according to the multi-stage conversion, which improves the power supply reliability of the hardware circuits. After test verification, the device has stable performance and high calculation accuracy, and the calculation error of each parameter is within 0.5%.

1 INTRODUCTION

In the 21st century, the rapid development of EMU speed and intelligence, and inevitably accompanied by the introduction of the corresponding high-power and nonlinear equipment, EMU asymmetric load and other nonlinear load capacity continues to increase, which brings a series of problems in the traction network system voltage and current waveform distortion, fluctuation and flicker, which seriously affects the power quality of the power supply system(Weiwei Li, 2020;Jianxiong Zhang, 2022;Ke Yin, 2020;Tao Liu, 2022). Therefore, it is urgent to conduct data monitoring on the power quality of the traction network during the operation of EMU, and use the data as support to trace and solve the problems, so as to provide guarantee for the safe operation of EMU(Liping Zhao, 2022;Guiping Cui, 2020;Zhuo Liu, 2021;He Wang, 2021;Shuang Yan, 2020).

At present, the power quality monitoring technology is mature in the field of power system, but because of the complex electrical coupling process of EMU train traction network, it is not suitable for the technical standards of power system(Guipeng Zhang, 2023). According to the survey, a unified and standardized standard system has not been formed in the field of EMU. The existing power quality monitoring device of traction network have single function, high cost, long development cycle time, and are mostly installed in traction substations. However, EMU trains as traction load are ignored as the incentive source of power quality deterioration of traction network. Therefore, the power quality of traction network should be monitored by monitoring the output signals of on-board voltage and current transformer of EMU(Yifeng Su, 2021;Qiang Li, 2021;Chengyue He, 2021;Shenggao Gong, 2020).

China National Railway Group Corporation Science and Technology Research and Development Program(N2022J008)

Zhang, J., Liu, Z., Guan, C., Ha, D. and Xiang, S.
Power Quality Monitoring Device of EMU Traction Network Based on Zynq.
DOI: 10.5220/0012876500004536

In *Proceedings of the 1st International Conference on Data Mining, E-Learning, and Information Systems (DMEIS 2024)*, pages 46-52
ISBN: 978-989-758-715-3

In summary, the XC7Z045 chip of Zynq-7000 series is selected as the main control chip, and a monitoring device is built with AD9251 and other auxiliary chips to monitor the power quality of the traction network of the EMU by monitoring and recording the voltage transformer, secondary voltage of current transformer and current output signals on the EMU. At the same time, the device adopts mature chip products for research and development, which has the advantages of low cost, fast development speed, perfect function and easy expansion. This paper introduces the design principle of power quality monitoring device, and verifies the accuracy and stability of the system by using standard power source.

2 OVERALL DESIGN SCHEME

The overall structure block diagram of the monitoring device is shown in Figure 1. It mainly includes the following four modules: signal acquisition module, signal processing module, data transmission module and power module. The signal acquisition module uses AD9251 analog-to-digital conversion chip to realize high-speed synchronous signal acquisition; Signal processing module uses dual-core ARM and FPGA embedded in XC7Z045 main control chip to realize high-speed data processing. The data transmission module uses 88E1116R Ethernet chip to construct gigabit network circuit to realize high-speed data transmission. The power module uses the DC-DC conversion chip and a series of voltage regulator chips to realize the normal operation of the device.

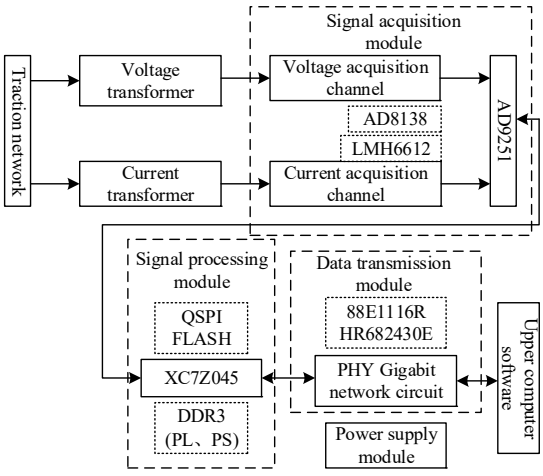

Figure 1: System structure diagram.

3 MAIN MODULE DESIGN

3.1 Signal Acquisition Module

The signal acquisition module is designed based on AD9251 analog-to-digital conversion chip. When the train is running in steady state, the net voltage RMS value is 17.5kV~31.5kV, and the voltage transformer ratio is 250:1, so the secondary voltage RMS value is 70V~126V. Since overvoltage faults often occur during train operation, and the peak value of overvoltage is high, in order to ensure that the system can withstand the overvoltage shock, the maximum voltage input is considered to be ±1250V, thus the voltage acquisition channel circuit design is carried out. Moreover, the voltage input range of the AD9251 chip in the signal acquisition module is ±1V. Considering this, a resistive-capacitive (RC) voltage divider circuit with a turns ratio of 1000:1 is designed. This circuit reduces the high voltage signal with a peak value of 1250V to 1.25V. To minimize the impact introduced by the monitoring device, the input impedance of the monitoring device needs to be designed to be greater than 1MΩ. In order to ensure stable turns ratio over a wide frequency range, the RC voltage divider circuit needs to satisfy Equation 1, where R_1 and R_2 represent the resistances of the high and low voltage arms, and C_1 and C_2 represent the capacitances of the high and low voltage arms. As shown in Figure 2, the high voltage arm of the voltage divider circuit consists of four 1MΩ resistors connected in series. The low voltage arm is constructed by connecting a 150KΩ resistor in series with a 5.1KΩ resistor, and then these are connected in parallel with a 4.3KΩ resistor. This configuration forms a 1000:1 voltage divider circuit. After the step-down circuit is the voltage following circuit composed of the integrated operational amplifier model LMH6612MA, where the 100Ω and 390Ω resistors form a voltage divider circuit, making the circuit gain 0.796. Thus, the large voltage signal with the maximum peak value of 1250V is converted into a small voltage signal with the peak value of 1V after a series of step-down processing.

$$\frac{R1}{R2} = \frac{C2}{C1} \quad (1)$$

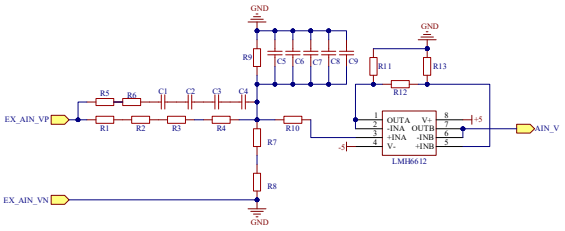

Figure 2: Voltage acquisition circuit schematic.

When the train is running in steady state, the RMS of the network current is 480A~720A, and the transformer ratio is 600:1, so the RMS of the secondary side current is 0.8A~1.2A. In order to ensure that the system current acquisition has a certain margin, the maximum current input is considered to be ±2.5A, so the current acquisition channel circuit is designed. As shown in Figure 3, the current sampling resistors are two high-precision cryobleach 0.05Ω resistors in series to convert a ±2.5A current signal into a ±0.25V voltage signal. Then the voltage signal of ±0.25V passes through the integrated operation amplifier of model LMH6612MA to form a voltage amplifier circuit with gain of 3.9, amplifies the voltage signal of ±0.25V to a voltage signal of ±1V, and outputs it to the rear circuit. The gain calculation formula for the current sensing circuit shown in Figure 3 is given by Equation 2, where R_{19} = 390Ω and R_{18} = 100Ω. From this, we can calculate the gain to be 3.9.

$$\text{Gain} = \frac{R19}{R18} \tag{2}$$

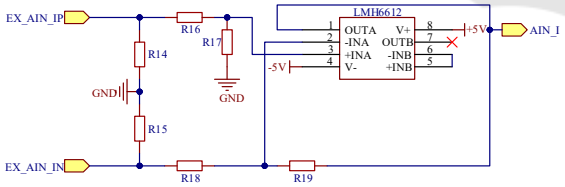

Figure 3: Current acquisition circuit schematic.

The signal acquisition module of the monitoring device uses AD9251 chip for signal acquisition. The AD9251 is a single-chip, dual-channel, 14-bit ADC acquisition chip powered by a 1.8V analog power supply that supports differential analog signal inputs up to 2Vpp, with high signal-to-noise ratio (SNR), large spury-free dynamic range (SFDR), and low power consumption. Integrated with a high-performance sample-and-hold circuit and an on-chip reference voltage source, the sample-and-hold circuit can maintain stable and excellent performance at input frequencies up to 200MHz. The chip uses a multistage differential pipeline architecture with integrated error correction logic to provide 14-bit accuracy and guarantee no code loss over the entire operating temperature range. Since the input signal is a differential analog signal, and the output of the acquisition channel circuit is a single-ended signal, it is necessary to add a single-ended to differential circuit after the acquisition channel circuit to drive the ADC. At the same time, because the voltage and current acquisition channels both output voltage signals of ±1V, the single-ended to differential ADC driving circuits of the two channels are exactly the same. The circuit schematic diagram is shown in Figure 4. The low-distortion differential ADC driver AD8138 is used to complete the circuit principle design, and the output end is connected to the signal input port of the AD9251. This drives the ADC for data acquisition. Figure 5 shows the schematic diagram of the AD9521 peripheral circuit, which mainly includes clock circuits, including external reference clock input, clock frequency division circuit and clock synchronization circuit. The power supply circuit mainly includes analog power supply and digital power supply, wherein AVDD is analog power supply and DRVDD is digital output drive power supply, both of which are 1.8V, in which a plurality of 10μF large capacitors and 100nF small capacitors are incorporated for voltage regulation filtering; The input circuit mainly includes two differential signal input circuits, A and B. The output end of the voltage and current single-ended to differential circuit is connected to the port respectively to drive the ADC to collect voltage and current. The output circuit mainly includes data output and clock output; The control circuit mainly includes control SPI interface, control register and status register, and the AD9251 is configured and controlled through SPI interface.

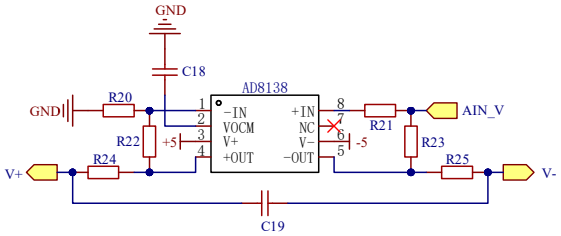

Figure 4: Single terminal to differential circuit schematic.

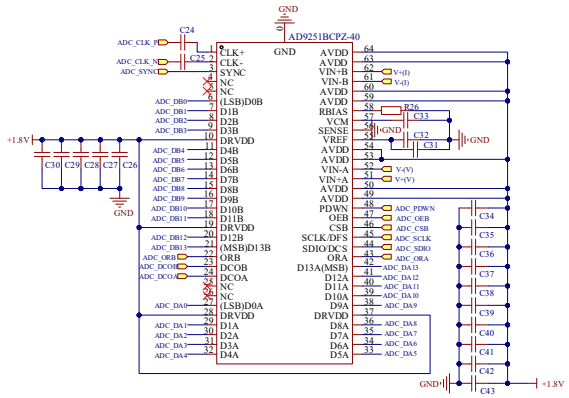

Figure 5: AD9251 peripheral circuit schematic.

3.2 Signal Processing Module

The XC7Z045 chip of Zynq-7000 series is the main control chip of the monitoring device. It is an SoC chip, which integrates the dual-core ARM Cortex-A9 processor and Xilinx 7 series FPGA. It has rich resources and communication interfaces, which is convenient for developers to expand and develop, and its working frequency is up to 1GHz. Data processing speed is fast. The monitoring device will carry out data calculation and analysis for each cycle signal, and package the calculated results and upload them every 100ms. At the same time, the original data will be packaged and uploaded at different sampling rates. The large amount of data requires high data processing speed of CPU. XC7Z045 is selected as the main control chip to make full use of its high computing speed.

The signal processing module mainly uses the FPGA contained in the main control chip to complete data processing, and uses the ARM contained in it to complete the configuration management and external communication of the device. In this paper, the monitoring device uses 10Msps sampling rate for original data acquisition, and 12.8K/S rate for data extraction (256 data points per cycle) for the calculation of power quality parameters, including voltage and current RMS. Frequency; Active, apparent and reactive power; Power factor; Dc offset; Voltage deviation; Voltage fluctuation; Voltage and current harmonics (up to 65 times); Voltage, current waveform distortion and other parameters. Every cycle, all parameters except harmonics and voltage fluctuation parameters are calculated, and every 100ms (5 groups of data are averaged) are packaged and uploaded. The harmonic parameters are calculated every 100ms, and the data of each harmonic component is packaged, and the voltage fluctuation parameters are calculated every minute. The data of each parameter is calculated and packaged in FPGA, and then transmitted to ARM. In ARM, network data is transmitted through TCP protocol.

3.3 Data Transmission Module

As shown in Figure 6, this system builds gigabit Ethernet circuit for data communication, selects 88E1116R Gigabit Ethernet chip for Ethernet circuit construction, and HR682430E network transformer chip for output isolation. 88E1116R chip supports 1.8V and 1.2V power supply, is a low-power 10/100/1000Mbps Ethernet chip, it integrates the MDI interface terminal resistor, eliminates 12 passive devices, reduces the complexity of peripheral circuits, And its reference clock supports 25MHz±50ppm tolerance crystal reference or oscillator input, reducing development costs. At the same time, it also has the following features: support for full duplex and half duplex mode, support for IEE 802.3u adaptive rate negotiation, support for IP\TCP\UDP uninstall acceleration, support for MAC address filtering and broadcast storm suppression.

3.4 Power Supply Module

The power module is responsible for the power supply of the entire hardware system. In this paper, the hardware system uses DC power supply for power supply, and several power management chips are selected to convert the voltage into the power supply voltage required by each module chip. The power supply logic diagram is shown in Figure 7. The transient voltage suppression diode (TVS) of model AMPA36CA is connected at the overall power input end of the hardware system to protect the overvoltage of the power supply end of the hardware system. The operating voltage of TVS of this model is 10-36V, so the overall power supply range of the hardware is DC10-36V. After TVS is the model TPS54560 DC-DC step-down chip, which is used to convert the input DC10~36V voltage into DC8V, and then use the power management chip to convert step by step, and finally output the power supply voltage required by each module.

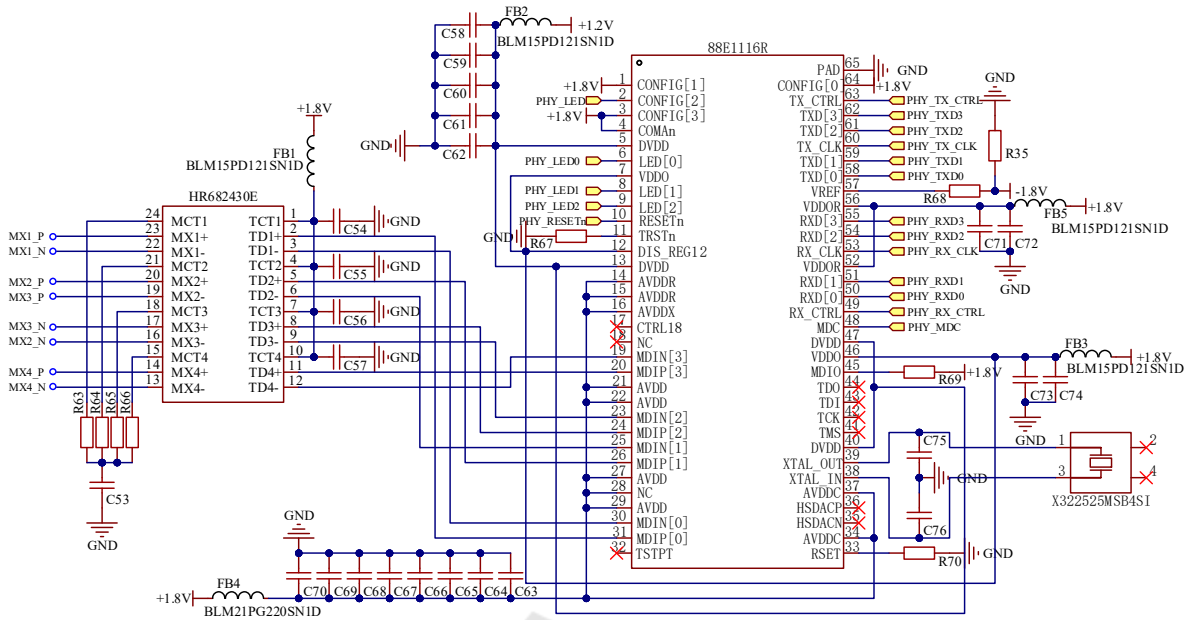

Figure 6: Gigabit ethernet transcelver and network transformer circuits.

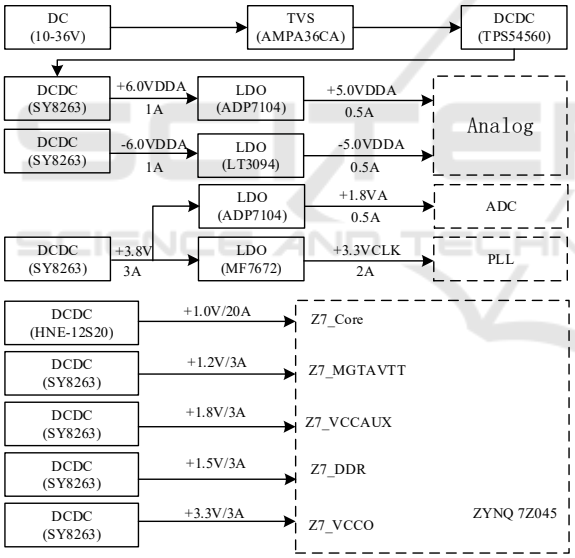

Figure 7: Power supply logic diagram.

4 SOFTWARE DESIGN

In order to visualize the data of the monitoring device and facilitate the user's use and management, it is necessary to develop the upper computer software. Qt Creator is a cross-platform graphical interface development platform that mainly supports C++ and Python languages. At the same time, Qt has a rich API, the library functions needed in the development process can be found in the API, and it also provides rich help documents, so that every developer can quickly get started, so Qt is widely used in GUI program development. In this paper, the host computer chooses the Windows version of Qt for software development, mainly realizes the data communication with the monitoring device, completes the configuration management, data display and data storage functions.

In this paper, the monitoring device and the host computer are located in the same LAN using gigabit network. The monitoring device is the server and the host computer is the client. In the TCP protocol, each server has its own IP address, and the client can only communicate with the server after searching for and connecting to the server's IP address. The running process of the host computer in this paper is shown in Figure 8. First, the UDP protocol is used to broadcast search for the IP address of the device in the LAN, and after searching for the IP address, it returns and connects to the TCP network port. After connecting the port, corresponding data is transmitted. Different packets transmit data through different network ports. Therefore, after the host computer successfully connects to the acquisition card, the port data needs to be analyzed according to the communication protocol, and the analyzed data is filled to the corresponding area for display. You can choose whether to store the data as required. If yes, the data is saved to a local folder and the file is named after the storage time.

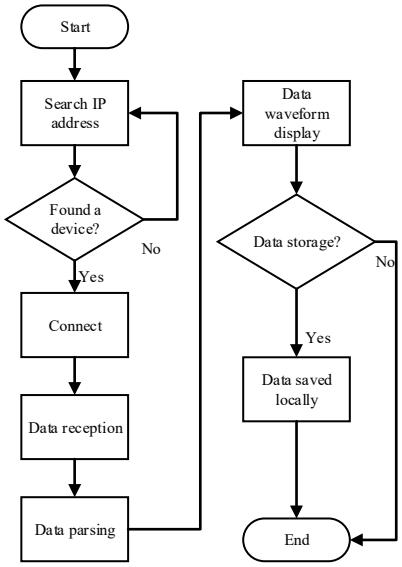

Figure 8: Upper computer software running flow.

In software interface design, Qt's built-in GUI interface class functions, such as QWidget, QGridLayout, QTableWidget, etc., and GUI component class functions, such as QPushButton, QLabel, QTextEdit, etc., are used to complete the overall design of the interface. Due to the presence of multiple ports for data transmission at the same time, the amount of data is large, so the response and processing speed of the upper computer software is particularly important, the use of multithreading can make better use of system resources, make full use of the idle time of the CPU, and use as little time as possible to make the system respond. Therefore, the design of the upper computer software of this system adopts multi-thread method for data processing. It can be roughly divided into receiving, parsing and display three threads, and use Qt's "signal and slot" mechanism to complete the data communication between threads, and the data communication process between threads is shown in Figure 9. First of all, after the host computer successfully connects the IP address of the acquisition card and the corresponding port in the data receiving thread, it uses the "readAll()" function in the QTcpSocket class to receive data, uses a byte stream object as the temporary cache of data, and then transmits the parsing signal, which will transmit the byte stream object. The parse slot function in the parse thread is called at this point. In the parsing slot function, the byte stream object in the signal is first received, and the semaphore is then released so that the parsing thread has resources to begin parsing the data. When the data is parsed, the data will be stored in the QVector container class object, and then the display signal will be transmitted, and the display signal will also be transmitted to the corresponding container class object. At this time, the display slot function in the display thread will be called. In the display slot function, the data in the container class object is first received, and then the data is filled into the corresponding area for display.

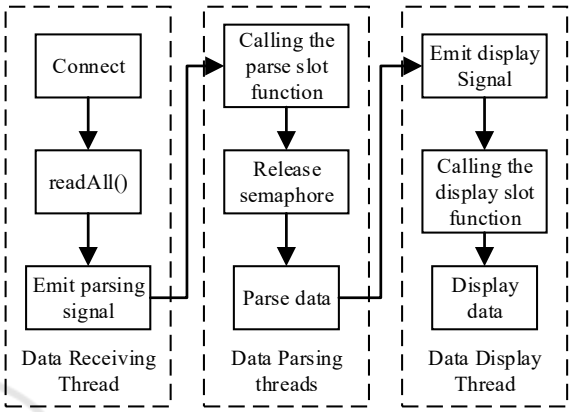

Figure 9: Data communication between threads.

5 TEST VERIFICATION

In order to verify the calculation accuracy of various parameters of the device, a three-phase standard power source STR3060A is used for experimental verification. The standard power is derived from basic parameters such as RMS value, frequency, power and harmonics of the output voltage and current that can be displayed in real time with a screen, with an accuracy of 0.5, and its single-phase sinusoidal output is connected to the monitoring system for precision comparison and verification. Set the fundamental voltage RMS value of 100V, the current RMS value of 1A, the third harmonic content of 20%, the fifth harmonic content of 5%, and the seventh harmonic content of 5%, adjust the fundamental frequency, and record and compare the total voltage and current distortion rate of the STR3060A and the monitoring device respectively. The test results are shown in Table 1.

The experimental results show that the maximum relative error of voltage RMS calculation is 0.15V, the maximum error of current RMS calculation is 0.007A, the maximum error of frequency calculation is accurate, the maximum error of total voltage distortion rate is 0.027, the maximum error of total current distortion rate is 0.033, and the total error is within 0.5%. It can be verified that the power quality

monitoring system designed in this paper can measure and calculate all parameters accurately.

Table 1: Parameter test results based on standard power sources.

	U_{RMS}/V	I_{RMS}/A	f/Hz	VTHD%	ITHD%
STR3060A	99.998	0.999	49.5	21.206	21.219
	99.998	0.999	50.0	21.213	21.214
	99.998	0.999	50.5	21.218	21.206
Device	99.848	1.006	49.5	21.190	21.239
	99.848	1.004	50.0	21.186	21.230
	99.848	1.006	50.5	21.190	21.239

6 CONCLUSIONS

This article presents the design of a traction power grid quality monitoring device for high-speed trains based on ZYNQ. The device utilizes the XC7Z045 chip from the ZYNQ-7000 series as the main control chip and is supplemented by other chips such as AD9251 to achieve overall functional design. It can analyze multiple power grid quality parameters. Through experimental comparison and verification, the device demonstrates parameter calculation errors within 0.5%, meeting the requirements for practical monitoring and accuracy. It also offers advantages such as low cost, fast development, complete functionality, and easy scalability. The device can be applied in the field of traction power grid quality monitoring for high-speed trains, providing reliable data support for safe operation and maintenance of the trains, and promoting the advancement of high-speed train technology.

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