HIERARCHICAL PERFORMANCE-ORIENTED CONTROL OF FLEXIBLE MANUFACTURING CELLS

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Abstract: In a job shop, each product may have a different processing route through the system. Automated Flexible Manufacturing Cells (FMC) that adopt this flow pattern are highly prone to deadlocks. A supervisor is a controller that uses available data via feedback loops to characterize the current behavior of the cell, and modify the equipment controllers to achieve the desired operational specifications in a deadlock-free manner. This paper proposes a hierarchical control system divided into an upper level scheduler and a lower level supervisor to control FMCs. The scheduler is responsible for determining a deadlock-free allocation of the resources that optimizes some performance measure, based on the current production requirements, and the supervisor guarantees that the flow plan (behavior) determined by the scheduler is realized on the shop floor. For that purpose, a formal method that can transform a production schedule into a supervisor, in real time, is also proposed. The supervisor is an augmented Marked Graph (MG) that captures all the events that can take place in the cell. The proposed approach is validated by generating and simulating the supervisors for two benchmark problems.

1 INTRODUCTION

Most automated manufacturing systems (AMSs) feature three inherent operational properties; mutual exclusion, no pre-emption, and the hold-while-wait property. Because of these conditions and the inherent flow complexities in job shop systems, when they are automated they become highly prone to deadlocks. A *deadlock* occurs in an automated manufacturing system when a set of jobs enter a *circular wait*, where each job continues holding (blocking) a system resource indefinitely while waiting for another resource to become available, which is in turn held by another job in this same set.

Scheduling and control of manufacturing systems have been widely researched and reported in literature in the past decades. However, a wide gap exists between the contributions found in the scheduling literature and those pertaining to actual implementation (supervision) on the shop floor (Sun et al., 2006). A few attempts, however, have been made to integrate deadlock-free scheduling and supervision, but these either lacked a global view of the system (Li & Jiang, 2006), or realized a poorer performance when compared to pure deadlock-free scheduling approaches.

In the previous literature, the Supervisory Control Theory (SCT) (Ramadge & Wonham, 1987) and Petri nets (PNs) have been the two most frequently used and commonly accepted methods by researchers for modeling and supervising AMSs. Limitations of the SCT approaches have been attributed to the large state space required to represent even small systems, and the complexity of analysis of the formal languages. On the other hand, PN literature on Supervisory Control (SC) can be classified into approaches that analyzed the Reachability graph of the net (Viswanadham et al., 1990, Hsieh & Chang, 1994) and approaches that characterized the deadlock states using siphons analysis (Ezpeleta et al., 1995, Chu & Xie, 1997). While the former approaches suffered either from the state explosion problem or the restrictiveness of the PN model (Fanti & Zhou, 2004), the latter ones suffered from the exponential complexity of determining the siphons of the net.

Automata and PN SC approaches have usually been combined with conventional scheduling

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approaches to solve the deadlock-free scheduling problem (Liljenvall, 1999, Golamakni et al., 2006, Lee & DiCesare, 1994, Ben Abdallah et al., 2002). However, these approaches have suffered from the same complexities which their SC counterparts have suffered from. To cope with these complexities, some heuristic approaches have been introduced to the literature to solve the problem. These included the work proposed in Huan & Wu (2004), Mati et al. (2001), and Fahmy et al. (2008). Others proposed mathematical formulations that can be solved to attain the optimal solutions for the problem (Ramaswamy & Joshi, 1996).

Nevertheless, the literature still lacks a formal approach that can transform a deadlock-free schedule of a job shop system into an implementable supervisor. The existence of such an approach would guarantee the correct and performance-optimized behavior of the system.

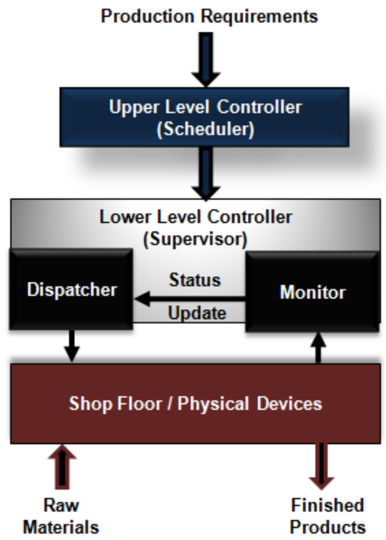

Figure 1: Proposed hierarchical control system.

2 HIERARCHICAL CONTROL

The type of systems considered is Flexible Manufacturing Cells (FMCs) that feature a job shop flow pattern. Such cells usually comprise a number of CNC machines that are served by a dedicated material handler (like a robot manipulator). In addition, they usually include some buffer capacity that can be used to temporarily store a job to preserve the continuity of flow or to resolve a deadlock.

Ideally, the functions of a production control system can be classified into three distinct functional modules; a scheduler, a monitor, and a dispatcher. Accordingly, a hierarchical control system divided into an upper level scheduler, and a lower level supervisor that monitors and dispatches commands to the shop floor (Figure 1) is proposed. According to the current product mix, the scheduler allocates processing slots for the jobs on the available machines while optimizing an objective criterion. The schedule further ensures that the resulting job flow cannot cause any deadlock situations. The assigned processing slots, and hence the underlying flow plan of the schedule is *transformed* into a supervisor. The supervisor will guarantee that the flow plan (behavior) determined by the scheduler is realized on the shop floor. The supervisor then interacts with shop floor devices by receiving feedback signals and accordingly issuing action commands directly from/to the shop floor.

3 SUPERVISOR REALIZATION

PN supervisors embedding a Marked Graph (MG) structure can be easily verified for liveness and reversibility. A MG is an ordinary PN in which each place has exactly one input transition and one output transition. A MG is live (deadlock-free) if the net structure obtained by deleting all the places marked by the initial marking contains no circuits, and a live MG is also reversible (Campos et al., 1992). Accordingly, the proposed approach initially transforms a given deadlock-free schedule into a live and reversible MG.

Consider the schedule of three jobs on three machines shown in Figure 2.

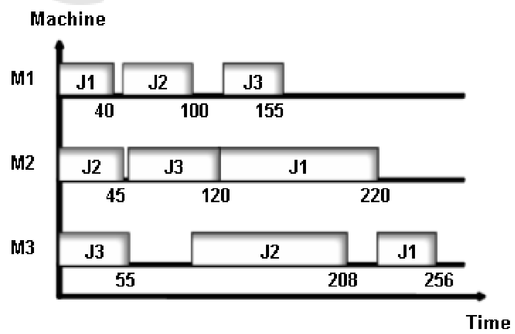

Figure 2: Schedule of illustrative example.

The first step to transform such schedule into a MG is to represent the processing route of each job by a production Petri net (PPN) (Banaszak & Krogh, 1990). This PPN provides the sequence of places and transitions that describe the flow of the job; places represent the processing operations, and transitions model the release and/or acquisition of the corresponding machine(s). A token in these places (*flow places)* indicates that a job is currently holding the corresponding machine, either while begin processed or while waiting for the next machine in its route. To represent the sequence of jobs visiting each machine as indicated by the schedule, each transition representing the release of a machine is connected to an additional place (*scheduling place*) by an input arc. This place is then connected by an output arc to the transition representing the acquisition of the same machine by the next visiting job. Accordingly, this machine will not be assigned to the next job until it is released by the current job (hold-while-wait condition). In order to ensure the initiation and repetition of the schedule, a token-occupied place is added between the transition that releases the machine from the last job in the visiting sequence, and the transition that acquires the machine for the first job in the sequence (Figure 3). Note that the resulting net is still a MG and will henceforth be referred to as a *scheduling marked graph* (SMG).

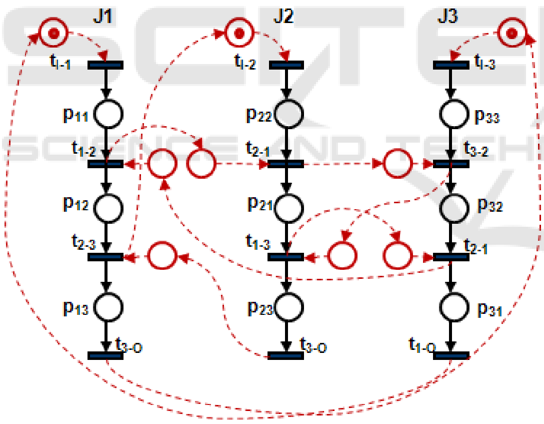

Figure 3: SMG of illustrative example.

The schedule shown in Figure 2 features a circular wait that would eventually result in a deadlock (Figure 3 contains three empty circuits). This circular wait can be resolved by placing J_1 in the buffer after completion on machine M_1, and hence expanding t_{1-2} into a flow place p_{1B} in-between two new transitions, t_{1-B} and t_{B-2}. A token in p_{1B} represents J_1 while residing in the buffer. Firing t_{1-B} releases M_1 and places J_1 in the buffer, while firing t_{B-2} acquires M_2 and moves J_1 from the buffer.

Using a hybrid approach earlier proposed in literature (DiCesare et al., 1993), through a series of top-down and bottom-up steps, the obtained SMG can then be augmented to represent the material handling (robot) operations while preserving the liveness and reversibility of the original SMG. Top-down decomposition first divides each flow place into two places with a transition in-between. The first place models the robot while handling the job and the second preserves the function of the original flow place. In order to ensure that the robot is not acquired simultaneously by more than one job, the bottom-up aggregation step adds a robot place p_R with one token to the SMG. This place is connected with output arcs to transitions that model the acquisition of the robot, and input arcs from transitions that model its release. After applying both steps, the augmented SMG (ASMG) can be obtained as shown in Figure 4. In this figure, arcs that connect p_R to its associated transitions are partially omitted and scheduling places along with their corresponding arcs are represented by bold arcs for the sake of clarity.

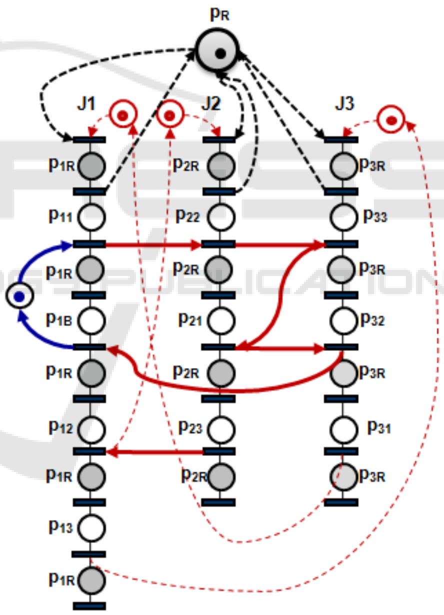

Figure 4: ASMG of illustrative example.

4 APPROACH VALIDATION

In order to validate the proposed approach, the supervisors for two benchmark problems are generated and simulated. Simulation entails executing the corresponding ASMGs of the problems to simulate the production process. The selected problems are the '4 jobs x 3 machines' problem introduced in Ramaswamy & Joshi (1996),

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and a ‘6 jobs x 6 machines’ problem that can be found in the OR library under the name *ft06*. The instance selected for problem ‘4J x 3M’ features a unit buffer capacity, and for problem ft06, no buffer space is available in the system. The times required to obtain the deadlock-free schedule using the heuristic proposed in Fahmy et al. (2008) and generate the corresponding ASMG for the 4Jx3M and *ft06* problems were 0.19 and 0.8 seconds, respectively. In order to test the reversibility of the supervisors, they were run for lot sizes of five parts for each job type. The two ASMGs were executed, and all the parts for all the job types for the two problems were completed successfully. The two ASMGs can now be implemented through a computer, which can be connected to cell devices to complete the required product mixes.

5 CONCLUSIONS

This paper has proposed an efficient hierarchical scheduling and control architecture for FMCs. The inputs to the proposed architecture are simply the available resources in the system and the production routes of the jobs to be produced. The output is a readily implementable supervisor, capable of driving the system to autonomously produce the required products in a deadlock-free manner, according to the best production schedule. The supervisor can further be updated in real time to accommodate any changes in the product mix, while preserving the optimized performance of the system. The output of this work can to some extent narrow the gap that exists between scheduling and control literature of AMSs.

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